REMARKS

Claims remaining in the present patent application are numbered 15-20. Claim 15 has been amended No new matter has been added. The rejections and comments of the Examiner set forth in the Office Action dated July 25, 2005 have been carefully considered by the Applicant. Applicant respectfully requests the Examiner to consider and allow the remaining claims.

35 U.S.C. §102 Rejection

The present Office Action rejected Claims 15-20 under 35 U.S.C. 102(e) as being anticipated by Kumar et al. (U.S. Patent No. 6,551,865). Applicant has reviewed the above cited reference and respectfully submits that the present invention as recited in Claims 15-20, is neither anticipated nor rendered obvious by the Kumar et al. reference.

Independent Claim 15

Independent Claim 1 recites that the present invention includes, in part:

> forming a first gate region at the bottom of said gate trench, said first gate region continuous in a lateral direction parallel to said surface;
>
> implanting a buffer region beneath said first gate; and
>
> implanting a second gate region beneath said buffer region, wherein said second gate region is

formed entirely beneath said first gate region, and wherein said second gate region is continuous in said lateral direction and is narrower than said first gate region . . . (Emphasis Added)

An embodiment of the present invention pertains to a method for fabricating a dual gate structure for a FET. In particular, embodiments of the present invention as described in independent Claim 15 describe the formation of a first gate region that is continuous in a lateral direction parallel to the surface of a semiconductor substrate. That is, first gate region is not separated by a gap. Further, embodiments of the present invention also disclose a second gate region that is formed beneath the first gate region. The embodiment of independent Claim 15 also describes the formation of a second gate region that is also continuous in the lateral direction, and is narrower than the first gate region. As such, the second gate region in the lateral direction parallel to the surface of the substrate does not extend beyond the first gate region.

Applicant respectfully notes that the prior art reference, Kumar et al., does not comprise nor suggest the formation of a dual gate FET structure that comprises the formation of a second gate region beneath a continuous first gate region, wherein the second gate region is narrower than the first gate region in the lateral

direction, as described in embodiments of the present invention as claimed in independent Claim 15.

The Kumar et al. reference discloses a silicon carbide semiconductor device with two gate regions that partially overlap in Figures 6 and 12. In particular, the FET of Figure 6 in the Kumar et al. reference describes the formation of a first gate region 7A and a second gate region 3. However, the second gate region 3 in the FET structure is not narrower than the first gate region 7A, which is in contrast to the claimed invention.

Furthermore, the FET of Figure 11 in the Kumar et al. reference describes the formation of a first gate region 7 in a FET structure. However, the first gate region in the Kumar et al. reference is not continuous in the lateral direction, which is in contrast to the claimed invention. Specifically, Figure 11 of the Kumar et al. reference illustrates the creation of the recess or gap region 8 that separates the first gate region into two portions in a lateral direction. That is, the Kumar et al. reference discloses a first gate region that is not continuous in a lateral direction.

On the other hand, the present invention distinctively recites the formation of a first gate region that is continuous in a lateral direction parallel to the top

surface of the semiconductor substrate, as recited in independent Claim 15. In particular, Figures 3B through 3F show the formation of a first gate region 320 without any recesses or gap regions in the lateral direction. This is in contrast to the Kumar et al. reference that discloses a formation of a first gate region including a recess or gap region in the lateral direction.

Additionally, the Kumar et al. reference describes the formation of a second gate region 3. As shown in Figure 2 of the Kumar et al. reference, the second gate region 3 is not formed entirely under a first gate region 7. That is, the second gate region 3 is formed under the recess or gap region 8 as well as the first gate region 7.

On the other hand, embodiments of the present invention disclose the formation of the second gate region entirely under the first gate region that is continuous in the lateral direction, as recited in independent Claim 15. In addition, embodiments of the present invention disclose the second gate region that is narrower than the first gate region in a lateral direction. That is, the second gate region is not formed under any recesses or gaps, as is described in the Kumar et al. reference.

Thus, Applicant respectfully submits that embodiments of the present invention as disclosed in independent Claim

15 are not anticipated nor rendered obvious by the Kumar et al. reference, and are in a condition for allowance. In addition, Applicant respectfully submits that Claims 16-20 which depend from independent Claim 15 are also in a condition for allowance as being dependent on an allowable base claim.

CONCLUSION

In light of the facts and arguments presented herein, Applicant respectfully requests reconsideration of the rejected Claims.

Based on the arguments presented above, Applicant respectfully asserts that Claims 15-20 overcome the rejections of record. Therefore, Applicant respectfully solicits allowance of these Claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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